

CLAIMS:

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1. A comparator, *comprising*: - a differential amplifier (M1, M2) having differential inputs (IN1, IN2) forming the comparator inputs, and a first and second amplifier output (Vo, Vo-) forming the comparator outputs of a first comparator stage,  
- a first differential current amplifier (A11) connected with its inputs to said amplifier  
10 outputs (Vo, Vo-) and connected with its output to said first amplifier output (Vo), and  
- a second differential current amplifier (A12) connected with its inputs to said amplifier outputs (Vo, Vo-) and connected with its output to said second amplifier output (Vo-).

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2. The comparator according to claim 1, *further comprising*  
a second comparator stage having an output amplifier (M5 – M10) whose inputs are  
connected to the comparator outputs (Vo, Vo-) of the first comparator stage and whose  
output forms the comparator output (OUT) of said second comparator stage.

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3. The comparator according to claim 2, *further comprising*  
switching means (M11) whose control input is connected to the comparator output  
(OUT) of the second comparator stage and whose control output is connected to the  
first output (Vo) of the differential amplifier (M1, M2).

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4. The comparator according to claim 3, *wherein*  
the switching means (M11) is a transistor.

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The comparator according to claim 3 or 4, *wherein*  
the switching means (M11) is connected to the output of the differential amplifier (M1,

M2) whose output signal needs longer to reach the comparator output (OUT) of the second comparator stage.

6. The comparator according to claim 3, 4 or 5, *wherein*
- 5 the switching means (M11) is in series connected to a current mirror transistor (M12), said current mirror transistor (M12) being provided to adjust a predetermined current ( $\alpha I_{tail}$ ) flowing through said switching means (M11).
7. The comparator according to any preceding claim, *wherein*
- 10 the differential amplifier comprises a first and a second input transistor (M1, M2) whose control outputs are connected to an auxiliary current source (Ibias).
8. The comparator according to claim 7, *wherein*
- 15 the auxiliary current source (Ibias) is connected via a current mirror (M19, M20) to the input transistors (M1, M2).
9. The comparator according to claim 8, *wherein*
- 20 the current mirror (M19, M20) is connected via a further current mirror (M21, M23) to the input transistors (M1, M2).
10. The comparator according to claim 9, *wherein*
- the auxiliary current source (Ibias) is connectable via a switching transistor (M18) to the current mirror (M19, M20).
- 25 11. The comparator according to claim 10, *wherein*
- the switching transistor (M18) is provided to be switched on, when the supply voltage (VDD) falls under a certain reference voltage ( $V_{thresh}$ ).